☐ 4. Document ID: US 6091863 A

L2: Entry 4 of 18 File: USPT Jul 18, 2000

DOCUMENT-IDENTIFIER: US 6091863 A
TITLE: Image processor and data processing system using the same processor

US Reference Patent Number (5):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6078337 A

L2: Entry 5 of 18 File: USPT Jun 20, 2000

DOCUMENT-IDENTIFIER: US 6078337 A
** See image for Certificate of Correction **
TITLE: Maintaining consistency of cache memory data by arbitrating use of a connection route by plural nodes

US Reference Patent Number (4):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 5893931 A

L2: Entry 6 of 18 File: USPT Apr 13, 1999

DOCUMENT-IDENTIFIER: US 5893931 A
TITLE: Lookaside buffer for address translation in a computer system

US Reference Patent Number (25):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 5812150 A

L2: Entry 7 of 18 File: USPT Sep 22, 1998

DOCUMENT-IDENTIFIER: US 5812150 A
TITLE: Device synchronization on a graphics accelerator

US Reference Patent Number (7):

5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 8. Document ID: US 5801720 A

L2: Entry 8 of 18 File: USPT Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5801720 A
TITLE: Data transfer from a graphics subsystem to system memory

US Reference Patent Number (4):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 9. Document ID: US 5793384 A

L2: Entry 9 of 18 File: USPT Aug 11, 1998

DOCUMENT-IDENTIFIER: US 5793384 A
TITLE: Image decoder with bus arbitration circuit

US Reference Patent Number (2):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 10. Document ID: US 5790134 A

L2: Entry 10 of 18 File: USPT Aug 4, 1998

DOCUMENT-IDENTIFIER: US 5790134 A
TITLE: Hardware architecture for image generation and manipulation

US Reference Patent Number (34):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 11. Document ID: US 5713043 A

L2: Entry 11 of 18 File: USPT Jan 27, 1998

DOCUMENT-IDENTIFIER: US 5713043 A
TITLE: Method and system in a data processing system for efficient determination of quality of service parameters

US Reference Patent Number (9):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Drawi Desc | Image

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☐ 12. Document ID: US 5680566 A

L2: Entry 12 of 18 File: USPT Oct 21, 1997

DOCUMENT-IDENTIFIER: US 5680566 A
TITLE: Lookaside buffer for inputting multiple address translations in a computer system

US Reference Patent Number (20):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Drawi Desc | Image

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☐ 13. Document ID: US 5675762 A

L2: Entry 13 of 18 File: USPT Oct 7, 1997

DOCUMENT-IDENTIFIER: US 5675762 A
TITLE: System for locking down part of portion of memory and updating page directory with entry corresponding to part of portion of the memory locked down

US Reference Patent Number (18):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Drawi Desc | Image

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☐ 14. Document ID: US 5675750 A

L2: Entry 14 of 18 File: USPT Oct 7, 1997

DOCUMENT-IDENTIFIER: US 5675750 A
TITLE: Interface having a bus master arbitrator for arbitrating occupation and release of a common bus between a host processor and a graphics system processor

US Reference Patent Number (6):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Drawi Desc | Image

☐ 15. Document ID: US 5664161 A

L2: Entry 15 of 18 File: USPT Sep 2, 1997

DOCUMENT-IDENTIFIER: US 5664161 A
TITLE: Address-translatable graphic processor, data processor and drawing method with employment of the same

US Reference Patent Number (4):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 16. Document ID: US 5649173 A

L2: Entry 16 of 18 File: USPT Jul 15, 1997

DOCUMENT-IDENTIFIER: US 5649173 A
TITLE: Hardware architecture for image generation and manipulation

US Reference Patent Number (34):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 17. Document ID: US 5553252 A

L2: Entry 17 of 18 File: USPT Sep 3, 1996

DOCUMENT-IDENTIFIER: US 5553252 A
** See image for Certificate of Correction **
TITLE: Device for controlling data transfer between chips via a bus

US Reference Patent Number (18):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 18. Document ID: US 5507026 A

L2: Entry 18 of 18 File: USPT Apr 9, 1996

DOCUMENT-IDENTIFIER: US 5507026 A
TITLE: Address-translatable graphic processor, data processor and drawing method with employment of the same

US Reference Patent Number (4):
5369744

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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